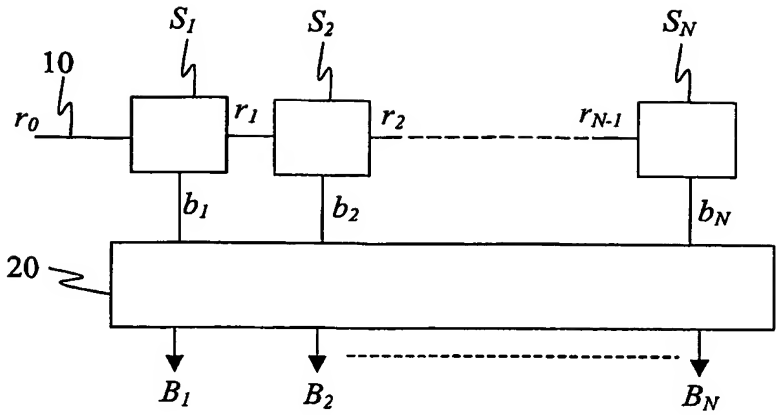

Fig. 1

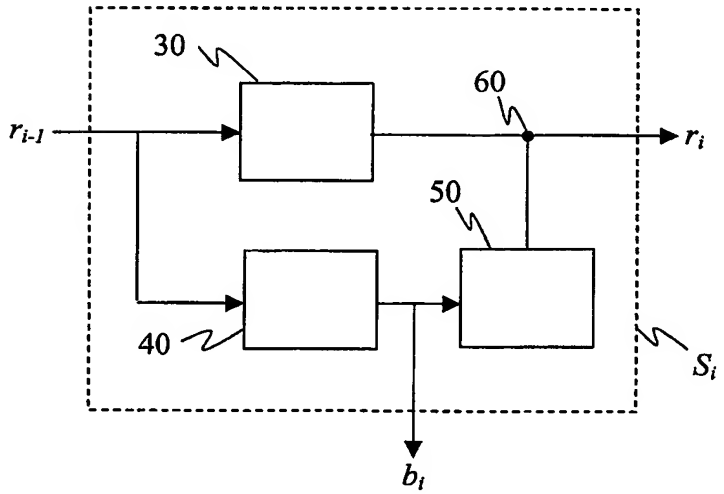

Fig. 2

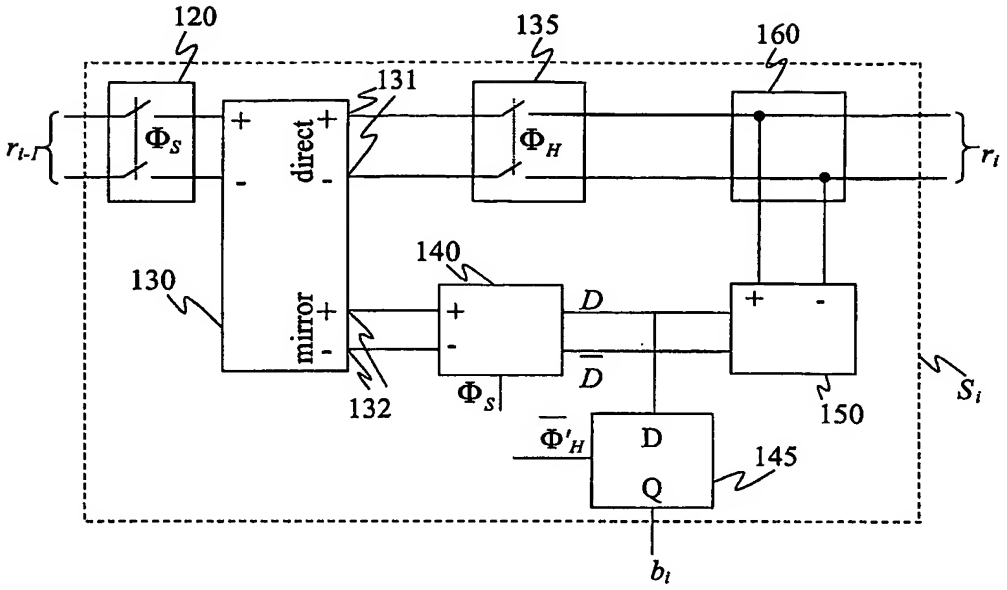
120
135
160
131
r_{i-1}
Φ_S
direct
Φ_H
r_i
140
130
mirror
D
$\overline{D}$
Φ_S
132
150
S_i
$\overline{\Phi'_H}$
D
Q
145
b_i

Fig. 3

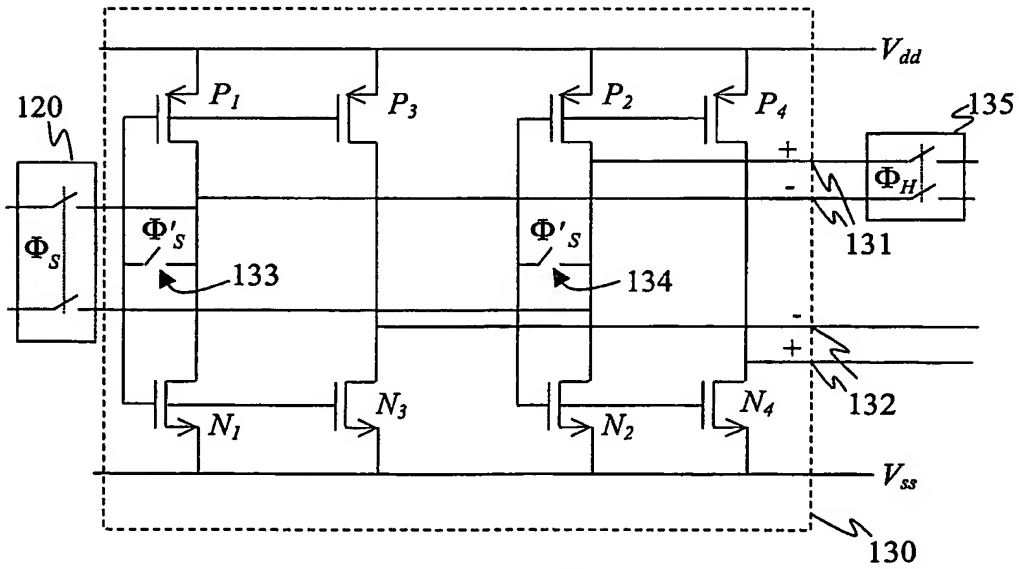
V_{dd}
120
P_1
P_3
P_2
P_4
135
Φ_S
Φ'_S
133
Φ'_S
134
Φ_H
131
132
N_1
N_3
N_2
N_4
V_{ss}
130

Fig. 4

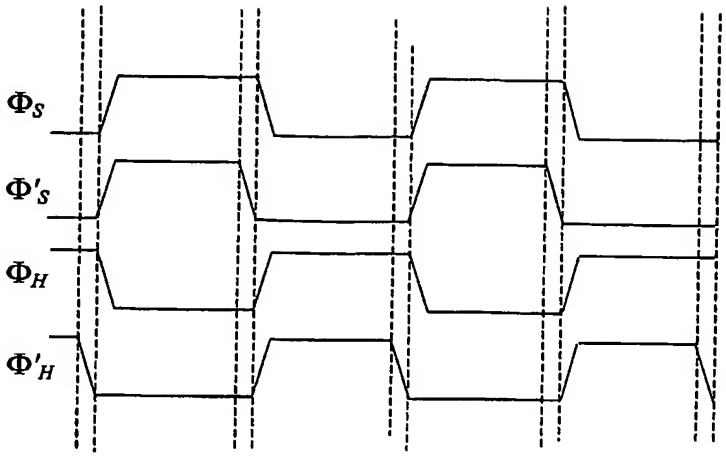
Φ_S
Φ'_S
Φ_H
Φ'_H

Fig. 5

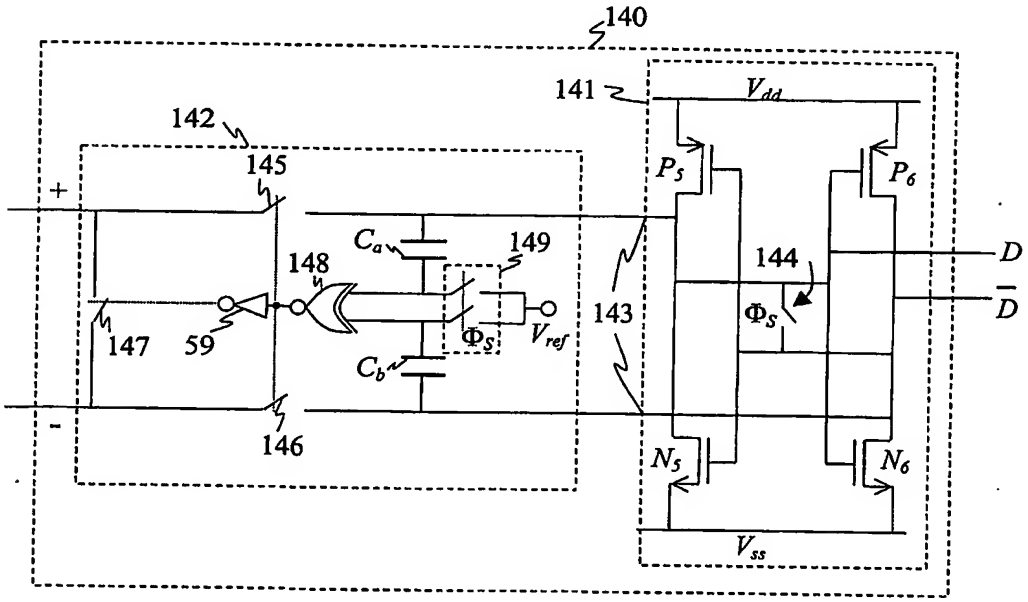
140
141
142
145
V_{dd}
P_5
P_6
+
C_a
149
148
144
D
$\overline{D}$
143
Φ_S
147
59
V_{ref}
C_b
-
146
N_5
N_6
V_{ss}

Fig. 6

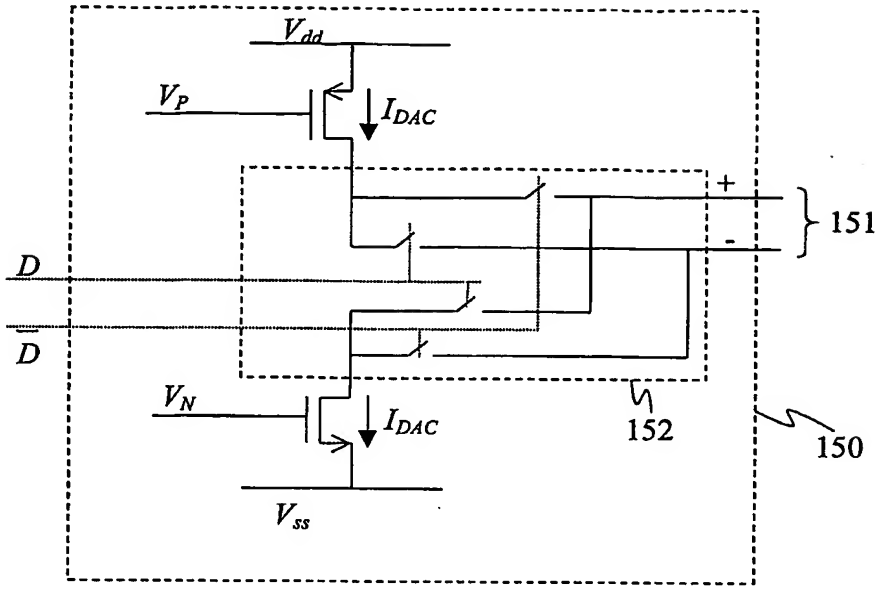
V_{dd}
V_P
I_{DAC}
+
-
151
D
$\overline{D}$
V_N
I_{DAC}
152
150
V_{ss}

Fig. 7

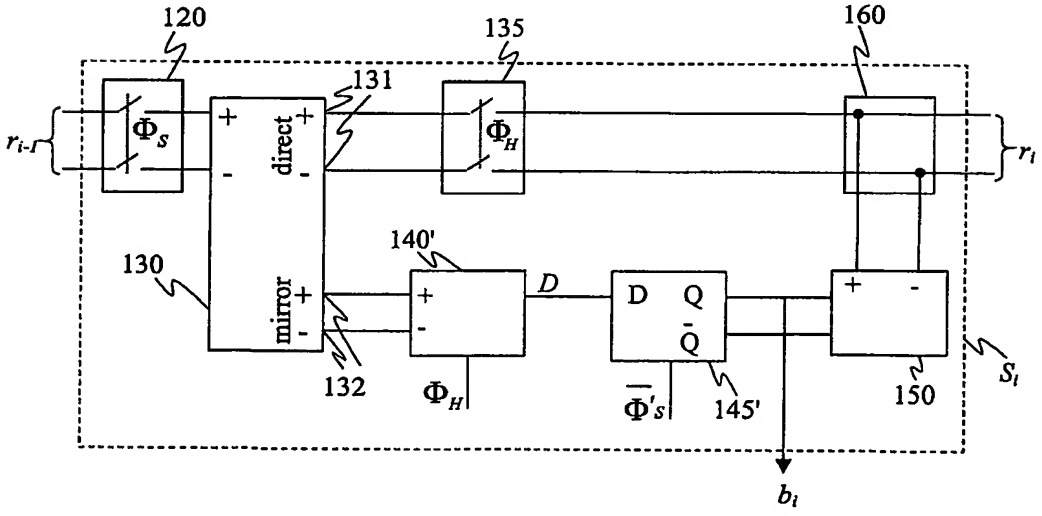
120
135
160
131
r_{i-1}
Φ_S
direct
Φ_H
r_i
140'
130
mirror
D
D Q
$\overline{Q}$
132
Φ_H
$\overline{\Phi}'_S$
145'
150
S_i
b_i

Fig. 8

10/521670

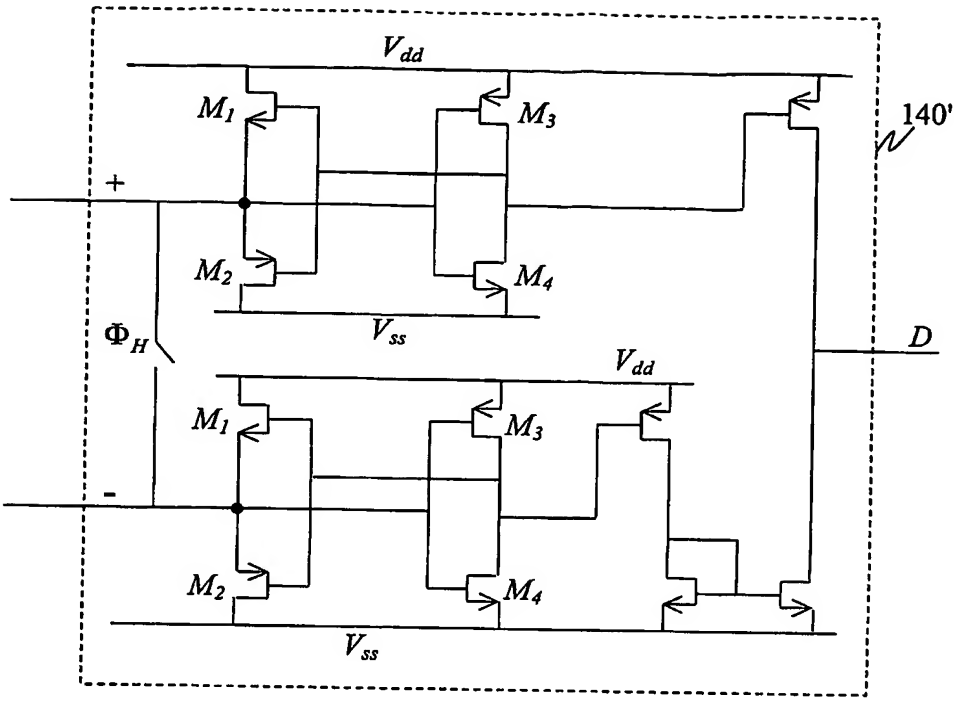

Fig. 9

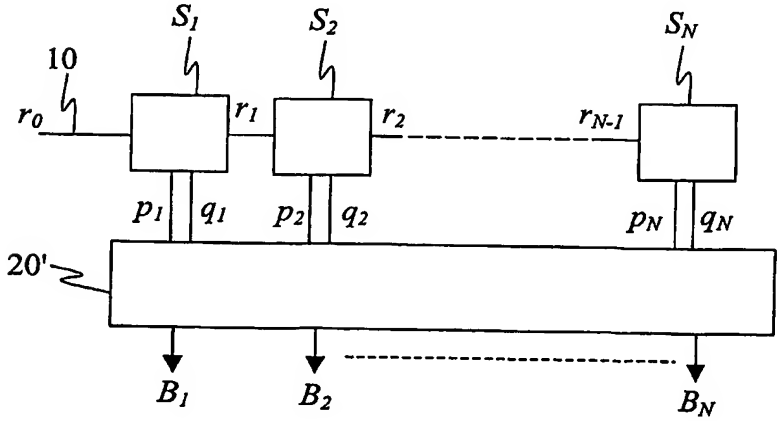

Fig. 10

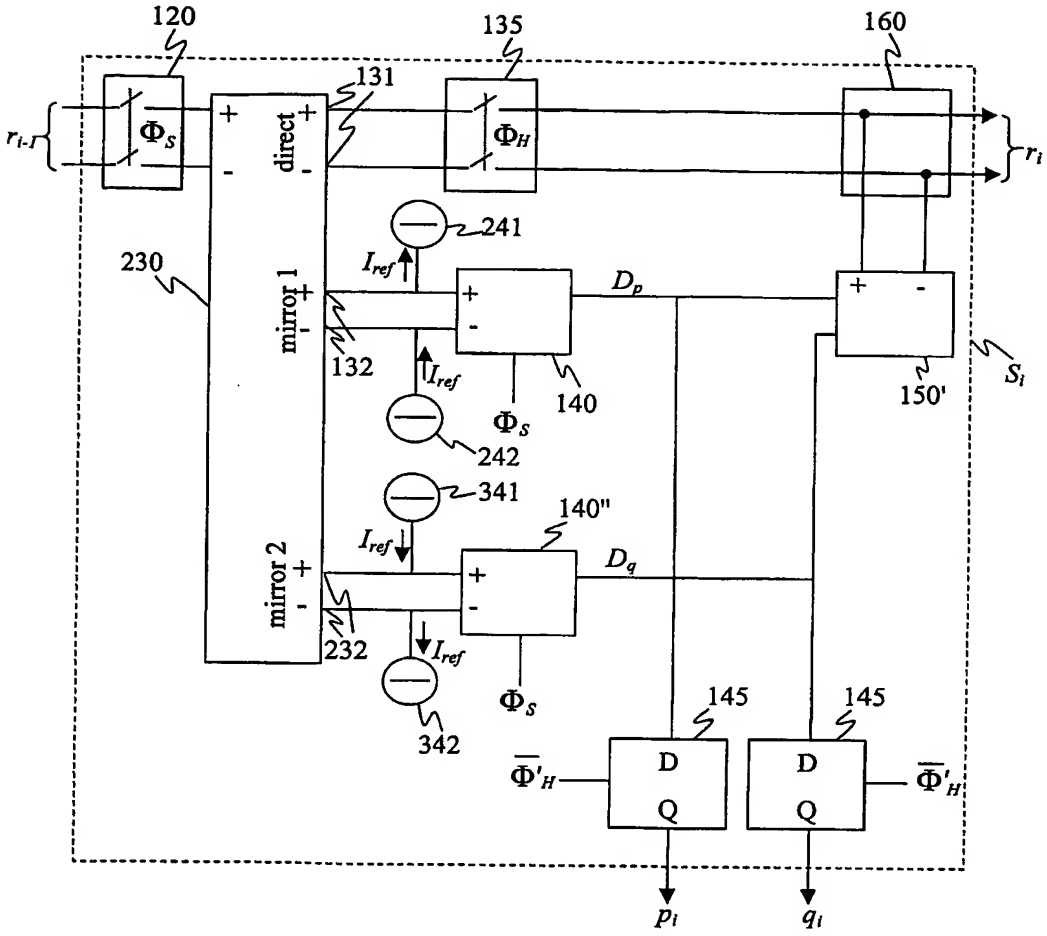
120
135
160
131
r_{i-1}
Φ_S
direct
Φ_H
r_i
241
230
I_{ref}
mirror 1
D_p
132
I_{ref}
140
150'
S_i
Φ_S
242
341
140"
I_{ref}
mirror 2
D_q
232
I_{ref}
Φ_S
145
145
342
$\overline{\Phi}'_H$
D
Q
D
Q
$\overline{\Phi}'_H$
p_i
q_i

Fig. 11

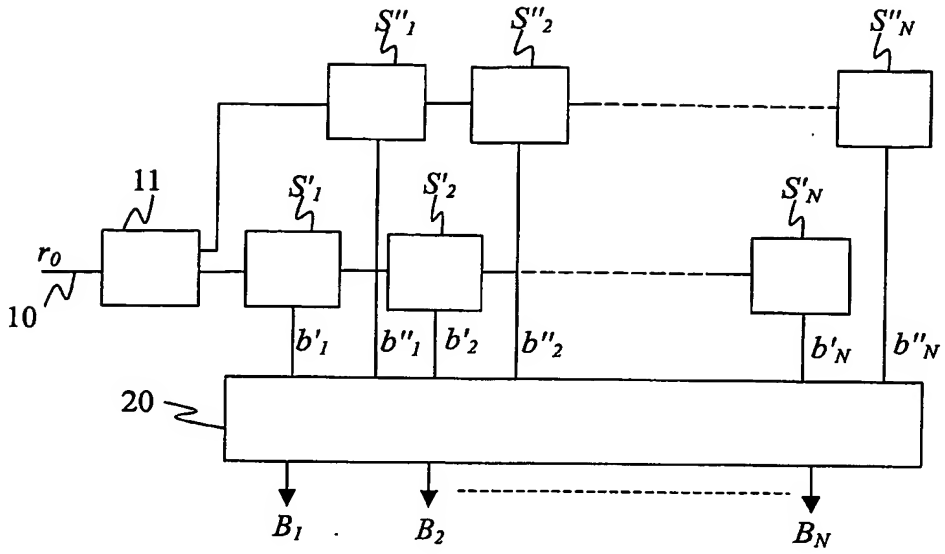
S''1
S''2
S''N
11
S'1
S'2
S'N
r0
10
b'1
b''1
b'2
b''2
b'N
b''N
20
B1
B2
BN

Fig. 12

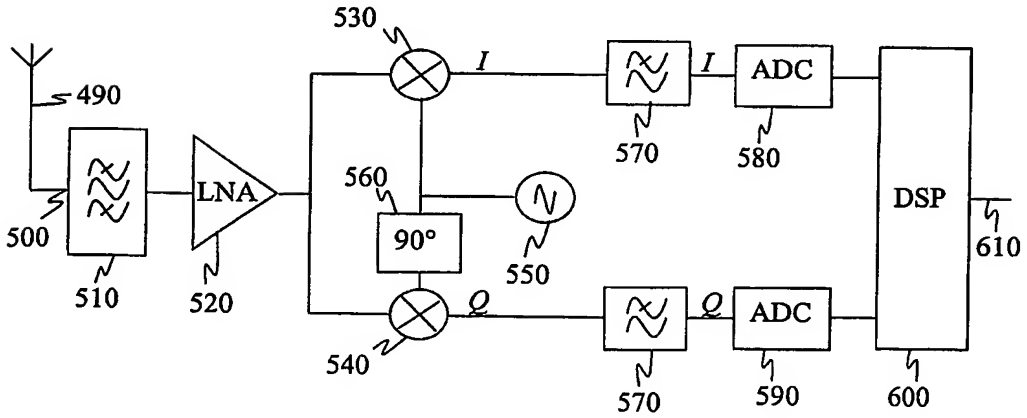
530
490
I
I
ADC
570
580
560
LNA
DSP
90°
550
500
510
520
610
Q
Q
ADC
540
570
590
600

Fig. 13

Conversion stage	Element	Clock Phase Φ_1	Clock Phase Φ_2
S_i odd i	Current memory means (130)	Sampling	Holding
	Comparator means (140)	Resetting	Quantising
	DAC (150)	OFF	ON
S_i even i	Current memory means (130)	Holding	Sampling
	Comparator means (140)	Quantising	Resetting
	DAC (150)	ON	OFF

Fig. 14

Conversion stage	Element	Clock Phase Φ_1	Clock Phase Φ_2
S_i odd i	Current memory means (130)	Sampling	Holding
	Comparator means (140')	Quantising	Resetting
	DAC (150)	OFF	ON
S_i even i	Current memory means (130)	Holding	Sampling
	Comparator means (140')	Resetting	Quantising
	DAC (150)	ON	OFF

Fig. 15

Conversion stage	Element	Clock Phase Φ_1	Clock Phase Φ_2
S'_i, odd i	Current memory means (130)	Sampling	Holding
	Comparator means (140)	Resetting	Quantising
	DAC (150)	OFF	ON
S'_i, even i	Current memory means (130)	Holding	Sampling
	Comparator means (140)	Quantising	Resetting
	DAC (150)	ON	OFF
S''_i, odd i	Current memory means (130)	Holding	Sampling
	Comparator means (140)	Quantising	Resetting
	DAC (150)	ON	OFF
S''_i, even i	Current memory means (130)	Sampling	Holding
	Comparator means (140)	Resetting	Quantising
	DAC (150)	OFF	ON

Fig.16

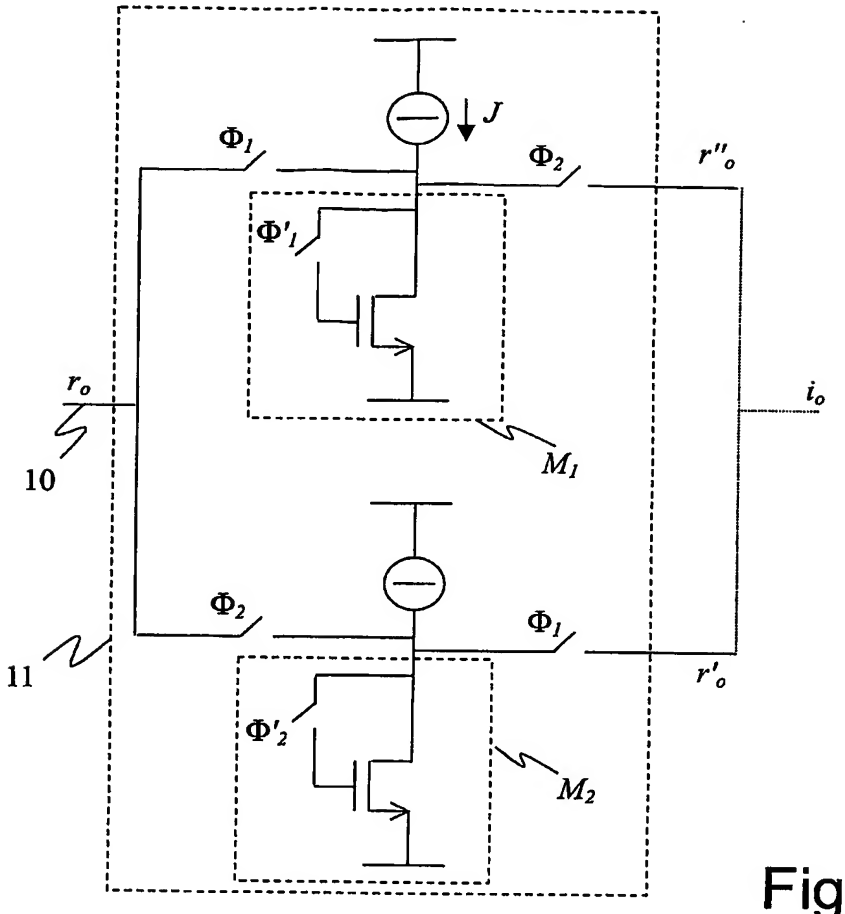

Fig. 17

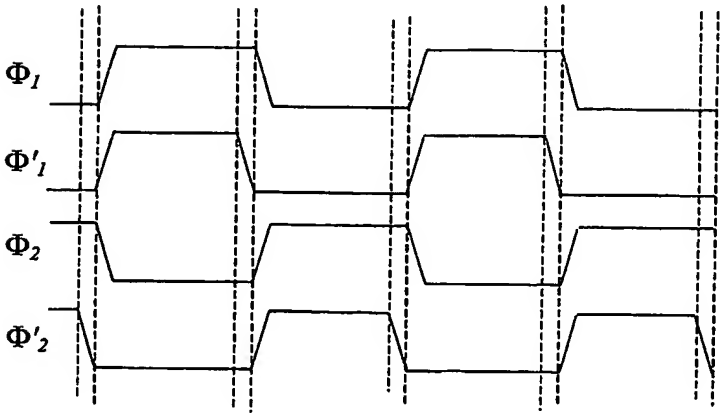

Fig. 18

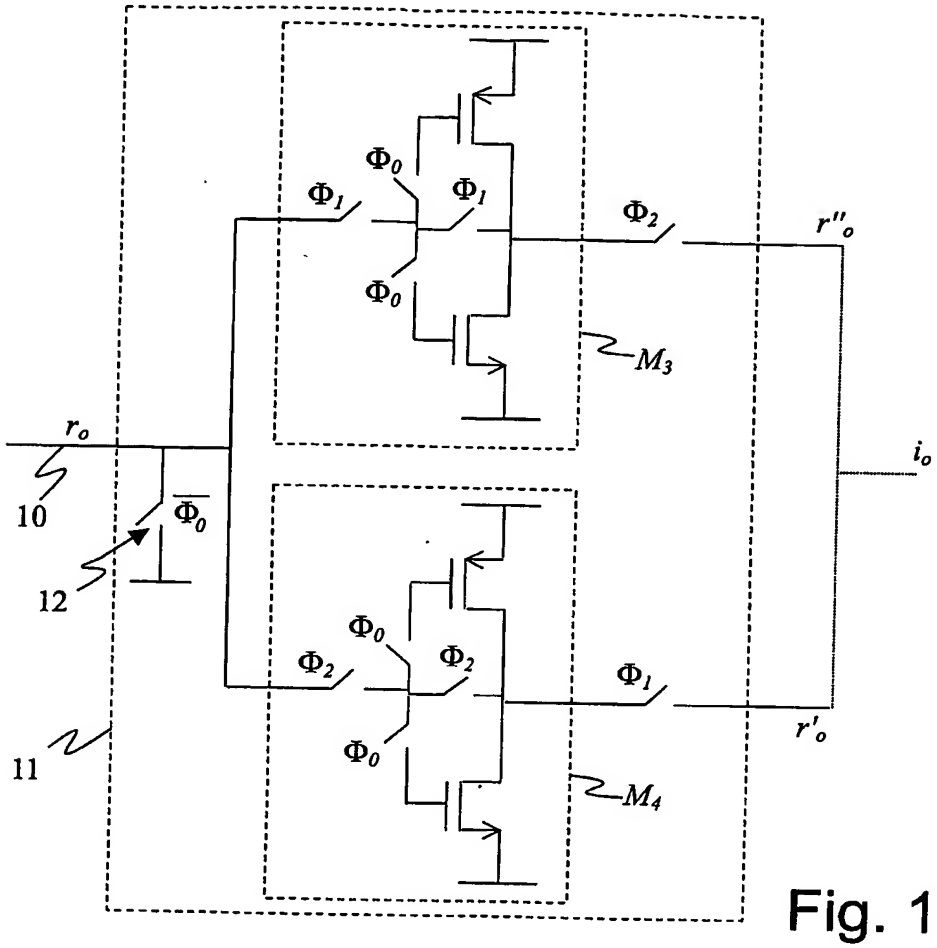
Φ_0
Φ_1
Φ_1
Φ_2
r''_o
Φ_0
M_3
r_o
i_o
10
$\overline{\Phi_0}$
12
Φ_0
Φ_2
Φ_2
Φ_1
r'_o
Φ_0
11
M_4

Fig. 19

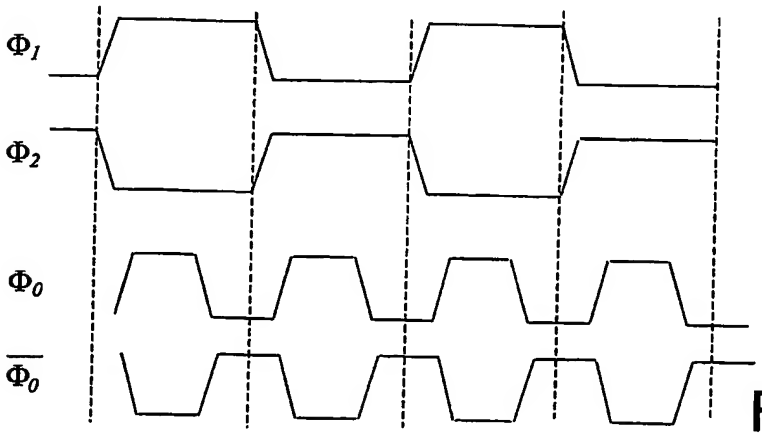
Φ_1
Φ_2
Φ_0
$\overline{\Phi_0}$

Fig. 20